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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,052	12/30/2003	Ian Graham Bolton	1801270.00138US1	7395

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WILMERHALE/BOSTON
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BOSTON, MA 02109

EXAMINER	
KISS, ERIC B	

ART UNIT	PAPER NUMBER
2192	

NOTIFICATION DATE	DELIVERY MODE
08/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/749,052	BOLTON ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-27,29-42,44 and 45* is/are rejected.

7)☒ Claim(s) *13,28 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20080328*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed March 28, 2008, has been received and entered. Claims 1-45 are pending.

Response to Amendment

2. The rejection of claims 3-15, 18-30, and 33-45 under 35 U.S.C. § 112, second paragraph, is withdrawn in view of applicant's amendments.

3. The rejection of claims 31-45 under 35 U.S.C. § 101 is withdrawn in view of applicant's amendments.

Response to Arguments

4. Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-12, 16-27, and 31-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Munehiro Takimoto and Kenichi Harada, "Partial Dead Code Elimination Using Extended Value Graph," 1999, Springer-Verlag, Lecture Notes in Computer Science, vol. 1694, proc. Of the 6th Int'l Symposium on Static Analysis, pp. 179-193 (prior art of record; herinafter "PDE1999").

Regarding claim 1, *PDE1999* discloses:

grouping together a plurality of basic blocks of the subject program code to form a group block (see, e.g., section 2, describing representing programs as a control flow graph over a set of basic blocks);

decoding the plurality of basic blocks of the subject program code in the group block (*Id.*);

generating an intermediate representation from said plurality of basic blocks of the subject program code in the group block, wherein the intermediate representation comprised nodes and links arranged as a directed acyclic graph representing expressions, calculations and operations performed by the subject program code, including one or more nodes representing a register definition by the subject program code (*Id.*);

performing a partial dead code elimination optimization on said intermediate representation to generate an optimized intermediate representation, wherein the partial dead code elimination optimization traverses the intermediate representation to create a liveness analysis indicating when the register definition represented by the one or more nodes is a partially dead register definition which is live in one path and dead in another path through the group block (see, e.g., section 4.2);

generating target code from said optimized intermediate representation (see, e.g., section 6); and

executing said target code on said target computing system (see, e.g., section 6).

Regarding claim 2, *PDE1999* further discloses the partial dead code elimination optimization being performed on the one or more of the basic blocks in the group block which end in non-computed branches or computed jumps (see, e.g., section 4.2).

Regarding claim 3, *PDE1999* further discloses the step of performing the partial dead code elimination comprising:

identifying the partially dead register definitions within the one or more basic blocks in the group block ending in non-computed braches or computed jumps (see, e.g., section 4.2);

marking child nodes of the one or more nodes relating to the identified partially dead register definitions to produce a set of partially dead nodes (see, e.g., section 4.2); and

performing a code motion optimization algorithm to generate an optimized intermediate representation providing an optimized order for generating target code with reference to the set of partially dead nodes (see, e.g., section 4.2).

Regarding claim 4, *PDE1999* further discloses the partially dead register definition identifying step comprising:

for a register definition in the respective basic block, performing liveness analysis of said register definition in successor basic blocks containing destinations of said non-computed branches or computed jumps (see, e.g., section 4.2); and

identifying said register definition as being partially dead if said register definition is dead in at least one successor basic block and live in at least one other successor basic block (see, e.g., section 4.2).

Regarding claim 5, *PDE1999* further discloses forming a set of identified partially dead register definitions (see, e.g., section 4.2).

Regarding claim 6, *PDE1999* further discloses applying a recursive marking algorithm to identify partially dead child nodes in the intermediate representation of the one or more nodes representing the identified partially dead register definitions (see, e.g., section 4.2).

Regarding claim 7, *PDE1999* further discloses the recursive marking algorithm identifying a node in the intermediate presentation as a partially dead child node by ensuring that the node is not referenced by either a live node or a node relating to a live register definition (see, e.g., section 4.2).

Regarding claim 8, *PDE1999* further discloses the recursive marking algorithm identifying partially dead child nodes as those nodes which are only referenced in the intermediate representation by other partially dead nodes or partially dead register definitions (see, e.g., section 4.2).

Regarding claim 9, *PDE1999* further discloses the recursive marking algorithm including the steps of:

determining a dead count for a child node, wherein the dead count is the number of partially dead nodes referencing the child node in the intermediate representation (see, e.g., section 4.2);

determining a reference count for the child node, wherein the reference count is the number of references to the child node in the intermediate representation (see, e.g., section 4.2); and

identifying a child node as a partially dead when its dead count equals its reference count (see, e.g., section 4.2).

Regarding claim 10, *PDE1999* further discloses the recursive marking algorithm further recursively identifying whether the child nodes of identified partially dead child nodes are also partially dead (see, e.g., section 4.2).

Regarding claim 11, *PDE1999* further discloses the code motion optimization algorithm comprising:

for each identified partially dead register definition,

determining a path of nodes in the intermediate representation for said partially dead register which are live (see, e.g., section 4.2),

discarding the nodes in the intermediate representation for said partially dead register definition which are dead (see, e.g., section 4.2), and

determining partially live paths of nodes in the intermediate representation for said partially dead register definition and moving corresponding nodes into said partially live paths, where the nodes in the partially live paths are partially dead nodes, further wherein a partially live path of nodes exists for each respective branch or jump (see, e.g., section 4.2).

Regarding claim 12, *PDE1999* further discloses each node in the intermediate representation including an associated variable which identifies with which partially live path of nodes it is associated (see, e.g., section 3).

Regarding claims 16-27 and 31-42, these are computer-readable storage media and computer apparatus versions of the claimed methods discussed above (claims 1-12). The use of such computer-readable storage media and computer apparatuses is inherent in implementing the system disclosed in *PDE1999* (see, e.g., section 6, describing experimental results), and all other limitations have been addressed as set forth above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14, 15, 29, 30, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over *PDE1999*, as applied above to claims in view of Alfred v. Aho, et al., "Compilers: Principles, Techniques, and Tools," 1988, Addison-Wesley, pp. 554-555 (hereinafter "Aho1988").

Regarding claims 14 and 15, although PDE1999 fails to expressly disclose the code motion optimization algorithm further preventing consecutive load and store operation in the intermediate representation from being moved into one of the partially live paths or performing a load-store aliasing optimization, *Aho1988* teaches that it is known during code optimization to remove redundant loads and stores (p. 554 ("Redundant Loads and Stores")), and therefore, it would have been obvious to one of ordinary skiull in the art at the time the invention was made to incorporate such a known optimization to gain its additional benefits.

Regarding claims 29, 30, 44, and 45, these are computer-readable storage media versions of the claimed methods discussed above (claims 14 and 15). The use of such computer-readable storage media and computer apparatuses is inherent in implementing the system disclosed in *PDE1999* (see, e.g., section 6, describing experimental results), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

Allowable Subject Matter

9. Claims 13, 28, and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric B. Kiss/
Eric B. Kiss
Primary Examiner, Art Unit 2192